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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/628,748	07/28/2003	Young-Kai Chen	100.2485	4860

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PRIEST & GOLDSTEIN PLLC
5015 SOUTHPARK DRIVE
SUITE 230
DURHAM, NC 27713-7736

EXAMINER	
RAO, SHRINIVAS H	
ART UNIT	**PAPER NUMBER**
2814	

DATE MAILED: 12/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/628,748	CHEN ET AL.	
	Examiner	Art Unit	
	Steven H. Rao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03/05/2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/30/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

The application as currently filed does not claim priority from any previously filed Application. Therefore the earliest available filling date is the U.S. filling date namely 10/30/2003.

Information Disclosure Statement

Acknowledgment is made of receipt of Applicant's Information Disclosure Statement (PTO-1449) filled on 10/30/2003.

The references on PTO 1499 submitted on 10/30/2003 are acknowledged. All the cited references have been considered. However the foreign patents and documents cited by applicant are considered to the extent that could be understood from the abstract and drawings.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim s 1- 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over .Miles et al. (U.S. Patent No.6,384,463, herein after Miles) and in view of Keri (U.S. Patent No. 5,861,656, herein after Keri).

With respect to claim 1 Miles describes a microelectronic apparatus having protection against high frequency cross talk radiation, comprising a planar insulating substrate, (Miles col. 1 lines 33-35, and col. 2 lines 60-63 it is noted that planar and insulating are defined in for e.g. at least in Specification page 8 lines 5 to 14 and insulating means reduced capability to conduct electrons and holed which any undoped semiconductor layer like Miles layer described in col. 1 lines 33-35 will satisfy) an active semiconductor electronic device located over a first region of said insulating substrate, (Miles fig.1 #2 or 4, col. 2 lines 30-35).

Miles describes a doped semiconductor (eg. figure 4 #22) without specifically describe the doped semiconductor as substantially surrounding the insulating substrate .

However Keri , a patent from the same filed of endeavor , describes in figure 3 and col. 2 lines 38 to 49 the doped semiconductor as substantially surrounding the insulating substrate to avoid rather complicated and extra circuit area and/ or processing steps in connection with manufacture but rather provide a simple manner wit reduced number of steps so as to protect devices in high voltage integrated circuits.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to include Keri's 49 the doped semiconductor as

substantially surrounding the insulating substrate in the place of Miles doped semiconductor . The motivation to make the above substitution is to avoid rather complicated and extra circuit area and/ or processing steps in connection with manufacture but rather provide a simple manner wit reduced number of steps so as to protect devices in high voltage integrated circuits.

With respect to claim 2. Miles describes the microelectronic apparatus of claim 1, in which said doped semiconductor is routed to ground. (Keri figures 1-4, etc. Miles col.2 lines 50-55, Keri col.3 lines 1-6)

With respect to claim 3 Miles describes the microelectronic apparatus of claim 1, in which said doped semiconductor fills a trench located in said second region. (Keri figures 1-4, #14,16,etc., Miles figure 3 # 8 in trench between trenches 16)

With respect to claim 4 Miles describes the microelectronic apparatus of claim 1, further comprising a dissipative conductor overlaying and adjacent to said doped semiconductor. (Miles figure 3 # 6 overlying and adjacent 8, Keri figure 3 #24 over and adjacent 14, 16)

With respect to claim 5 Miles describes the microelectronic apparatus of claim 1, further comprising: a second active semiconductor electronic device located over a third region of said insulating substrate, said third region being substantially separated from said first region by said second region. (Miles col. 1 lines 18-19).

With respect to claim 6 Miles describes the microelectronic apparatus of claim 1, in which said doped semiconductor comprises an n type semiconductor dopant.. (Miles col.3 lines 54-55).

With respect to claim 7 Miles describes the microelectronic apparatus of claim 4, further comprising a dielectric passivation layer having a first surface overlaying said insulating substrate and having a second surface, (Miles figures 3, 4 #16, Keri figures 18) said dielectric passivation layer having a thickness extending between said first and second surfaces; (inherent property of every layer to have a thickness) said dissipative conductor extending into said dielectric passivation layer. (Miles figure 3 # 8, Keri figures 14, 16 extending into 18)

With respect to claim 8 Miles describes the microelectronic apparatus of claim 4, in which the dissipative conductor is a metal. (Miles ring 6, col.2 line 44, Keri layer 24, col. 2 lines 50-51).

Wit respect to claim 9 Miles describes the microelectronic apparatus of claim 5, in which said first and second active semiconductor electronic devices are selected from the group consisting of transistors, circuits, integrated circuits, diodes, and memory cells. (Miles col.1 line17-18, Keri col.1 lines 6-7-i/cs, transistors)

With respect to claim 10 Miles describes the microelectronic apparatus of claim 7, in which said dissipative conductor fills a trench located in said dielectric passivation layer. (Miles figure 3 #8 between dielectric layers 16 , Keri figure 3 # 14,16 in trenches in passivation dielectric layer 18)

With respect to claim 11 Miles describes the microelectronic apparatus of claim 7, in which said dissipative conductor extends from said first surface toward said second surface over at least about half of said thicknessthe first and the second semiconductor substrates to be in different in their crystal plane orientation to increase stability of the

device increase productivity and enhance mechanical and electronic properties of the surface .

With respect to claim 12 Miles describes the microelectronic apparatus of claim 7, further comprising: metallic test probe contacts located at said second surface, said metallic test probe contacts making electrical connections with said active semiconductor electronic device. (Miles col. 2 lines 36-37)

With respect to claim 13 describes the microelectronic apparatus of claim l11, in which said dissipative conductor extends from said first surface to said second surface. the first and the second semiconductor substrates to be in different in their crystal plane orientation to increase stability of the device increase productivity and enhance mechanical and electronic properties of the surface .

With respect to claim 14 describes a method of making a microelectronic apparatus having protection against high frequency crosstalk radiation, comprising the steps of: providing a planar insulating substrate forming an active semiconductor electronic device located over a first region of said insulating substrate, and forming a doped semiconductor located in a second region of said insulating substrate substantially surrounding said first region. (Miles figure 3).

With respect to claim 15 Miles describes the method of claim 14, in which said doped semiconductor is formed by the step of implanting dopant ions in a trench located in said second region. (Keri figures 1-4, #14,16,etc., Miles figure 3 # 8 in trench between trenches 16)

With respect to claim 16 Miles describes the method of claim 14, further comprising the step of forming a dissipative conductor overlaying and adjacent to said doped semiconductor. (Miles figure 3 # 6 overlying and adjacent 8, Keri figure 3 #24 over and adjacent 14, 16)

With respect to claim 17 Miles describes the method of claim 14, further comprising the step of forming a second active semiconductor electronic device located over a third region of said insulating substrate, said third region being substantially separated from said first region by said second region. (Miles figure 1,col.2 lines 31-34)

With respect to claim 18 Miles describes the method of claim 16, further comprising the step of: forming a dielectric passivation layer having a first surface overlaying said insulating substrate and having a second surface; (Miles figures 3, 4 #16, Keri figures 18) said dielectric passivation layer having a thickness extending between said first and second surfaces; (inherent property of every layer to have a thickness extending between its two surfaces) said dissipative conductor extending into said dielectric passivation layer. (Miles figures 3,4 etc.)

With respect to claim 19 Miles describes the method of claim 18, in which said dissipative conductor is formed by the steps of: providing a trench located in said dielectric passivation layer; (Miles col. 3 lines 66-67, Keri figures and col.2 lines 22-30) and filling a dissipative conductor into said trench. (Miles figures 8 filled in tench col. 3 lines 66-67and Keri figures and col.2 lines 22-30)

With respect to claim 20 Miles describes the method of claim I 8, further comprising the step of: forming metallic test probe contacts located at said second

surface, (Miles ring 6, col.2 line 44, Keri layer 24, col. 2 lines 50-51) said metallic test probe contacts making electrical connections with said active semiconductor electronic device. (Miles figure 3and Keri figure3, col. 3 lines 20-25)

Any inquiry concerning this communication or earlier communication from the examiner should be directed to Steven H. Rao whose telephone number is (571) 272-1718 . The examiner can normally be reached on Monday- Friday from approximately 7:00 a.m. to 5:30 p.m.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 308-0956. The Group facsimile number is (703) 308-7724.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Steven H. Rao

Patent Examiner

December 09. 2004.